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Flexible Nonvolatile Transistor Memory Devices Based on One-Dimensional Electrospun P3HT:Au Hybrid Nanofibers

*Hsuan-Chun Chang, Cheng-Liang Liu, and Wen-Chang Chen**

A novel flexible nonvolatile flash transistor memory devices on polyethylene naphthalate (PEN) substrate using 1D electrospun nanofiber of poly(3-hexylthiophene) (P3HT):gold nanoparticles (Au NPs) hybrid as the channel is presented. The Au NPs are functionalized with self-assembled monolayer (SAM) of para-substituted amino (Au-NH_2), methyl (Au-CH_3) or trifluoromethyl (Au-CF_3) tail groups on the benzenethiol moiety. They are employed as localized charge traps across the nanofiber channel and program/erase the device towards low conductance (OFF)/high conductance (ON) states under the applied electrical field. With the low operation voltage of ±5 V, the hybrid nanofiber transistor memories exhibit a 3.5–10.6 V threshold voltage shifting and at least 10^4 s data retention, with a minimum effect on ≈100 programmed/erased stress endurances. The dipoles of the SAM probably modify the work function of the Au NPs associated with the P3HT nanofiber channel and manifest the degree of negative threshold voltage shifting in an order of Au-NH_2 > Au-CH_3 > Au-CF_3. The devices remain reliable and stable even under the bending conditions (radius: 5–30 mm) or 1000 repetitive bending cycles. The hybrid nanofiber can be used to obtain high-performance digital nanoscale memories for flexible high density data storage devices.

1. Introduction

Organic or polymeric-based switching memories are potential candidates for the emerging research memory technologies because they offer the advantages of flexibility for molecular design, low-cost and good processability with respect to inorganic counterparts.[1–8] Typical two-terminal resistor and three-terminal transistor memories are assembled to switch the device between the low/high conductance (OFF/ON) states associated with the volatility of storage devices. In particular, organic transistor memories have been developed in the information technologies including floating gate-, polymer electret- and ferroelectric-type organic field effect transistors (OFETs).[5–8] Hybrids of metal nanoparticles (NPs)/polymer materials were employed as charge trapping elements of transistor memories,[9,10] as a layer between thin tunneling dielectric and thick blocking dielectric,[11–14] or directly as polymer semiconductors channel.[15,16] Therefore, floating gate memory transistors with well-distributed metal NPs in charge trap layers allowed for modulating the high density memory device with discrete charge storage sites at a low voltage range.[10]

Nanoelectronics based on 1D nanomaterials (such as nanotube, nanowire or nanofiber) are considered to be promising candidates for the scaling-limiting problem in the semiconducting manufacturing technology.[17–19] Previous reports mainly based on 1D inorganic nanowires-based device1s decorated with metal NPs,[20–23] charge transfer molecules[24,25] or ferroelectric gate dielectric[26,27] were interacted as charge storage of floating gate transistor memories. Recently, our groups demonstrated larger threshold voltages shift of self-assembled n-type organic N,N'-bis(2-phenylethyl)-perylene-3,4:9,10-tetracarboxylic diimide (BPE-PTCDI) semiconducting nanowires for nonvolatile transistor memory applications due to its higher electrical field generated in the confined dimension.[27] Indeed, the 1D nanostructured conducting channel could increase the area density of device cells and also reduce the operating power consumption.

Electrospinning is a simple and versatile assembly technique for the direct growth of uniform and ultrafine 1D polymeric semiconducting nanofiber, with an enhanced carrier mobility and size-related intriguing physical properties.[29,30] Self-assembled monolayer (SAM) constructed by chemisorption of functional organic compounds to the metal NPs including addition of stability and prevention from agglomerating.[31] To incorporate the surface modified metal NPs into electrospun semiconducting polymer nanofiber can be used to explore the charge storage characteristics of nanoscale transistor memories. To the best of our knowledge, such 1D nanowire or nanofiber based module has been limited to inorganic nanowire memory storage and it has not yet been reported in flexible organic polymer floating-gate transistor memories.

Here, we report on the fabrication and characterization of transistor memories on flexible polyethylene naphthalate (PEN) substrate using the electrospun hybrid nanofiber prepared

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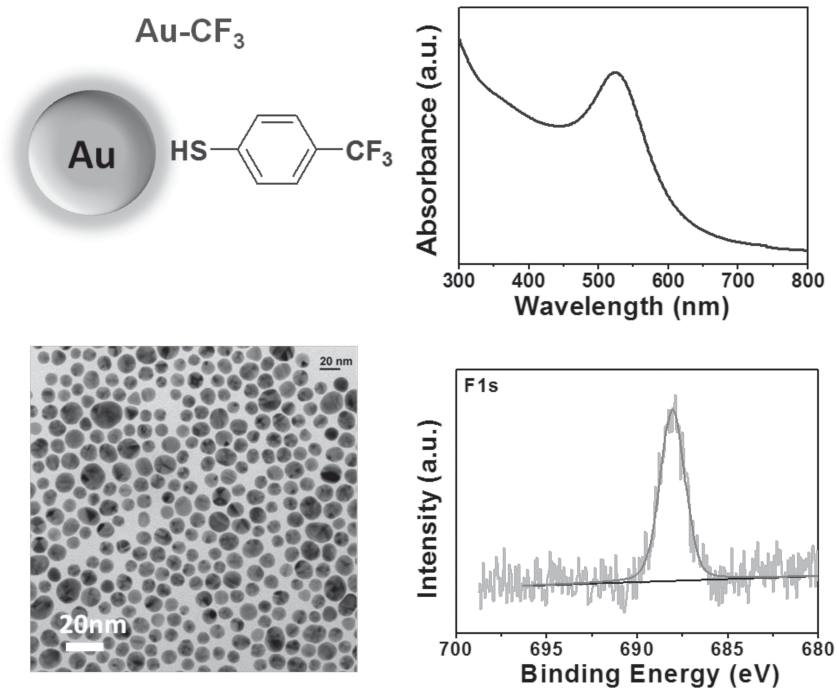

Figure 1. Representative plan-view TEM graphs, optical absorption spectra, and XPS analysis of the Au-CF_3.

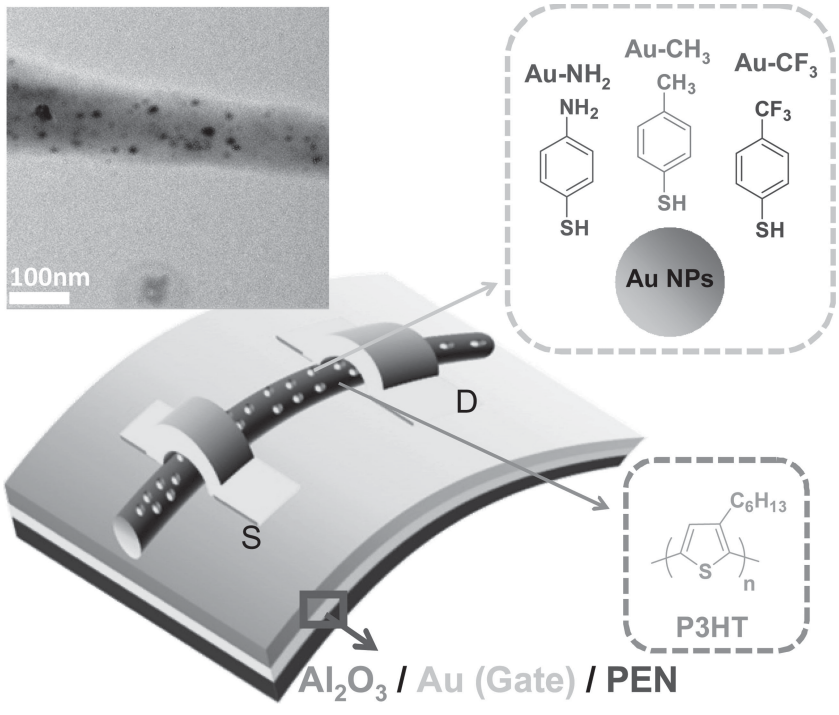

Figure 2. Schematic configuration of the hybrid nanofiber based transistor memory devices, chemical structures of P3HT and surface-modified Au NPs, and representative plan-view TEM measurements the P3HT:Au hybrid nanofiber.

from poly(3-hexylthiophene) (P3HT) semiconductor and SAM-modified Au NPs. The polarity of well-distributed Au NPs was tuned through wet chemical synthesis of cationic benzenethiol ligands attached on the NPs core[14,32] with different terminal electron-withdrawing trifluoromethyl group (Au-CF_3), electron-donating amino group (Au-NH_2) or electrically neutral CH_3 group (Au-CH_3), as shown in **Figure 1**. Incorporation of such uniform and high density NPs can be viewed as electric field-driven current modulator of three-terminal devices, where the charge trapping/detrapping process maintains the devices in ON/OFF state even under the bending condition. Excellent device performances including low operation voltages, retention and endurance ability as well as stability against external mechanical stimulus allow for it to be integrated in the future flexible logic circuits.

2. Results and Discussion

2.1. Characterization and Device Fabrication

The physical properties of the SAM-coated Au NPs in solution were verified by UV-Vis absorption spectra, X-ray photoelectron spectra (XPS) and TEM image (Figure 1; Figure S1, Supporting Information). The absorption spectra of Au NPs colloidal solution exhibits the strong peak centered at ≈525 nm. The functionalized NPs are nearly spherical with an average size of 15 ± 4 nm, calculated by collected TEM images including 22 isolated NPs (**Figure 2**). It indicates no significant change in Au NPs size and the aggregation is prevented by the SAM modification. Also, the head thiol ligands meet the requirement for lowering the free energy of the interface and makes Au NPs more stable.[30] To verify the tail groups on the surface ligands, the nature on chemical composition of the end functional groups is probed by XPS. Single F 1s, N 1s, and C 1s signals of Au-CF_3, Au-NH_2 and Au-CH_3 are observed at 687, 399 and 285 eV, respectively, suggesting the specific chemisorbed groups of the SAM coverage on the Au NPs surface.

Figure 2 illustrates prototypical electrospun P3HT/Au hybrid nanofiber-based transistor memories on a PEN substrate with a bottom-gate top-contact configuration using thermally evaporated Au as a back gate. Atomic layer deposition (ALD) of high-*k*

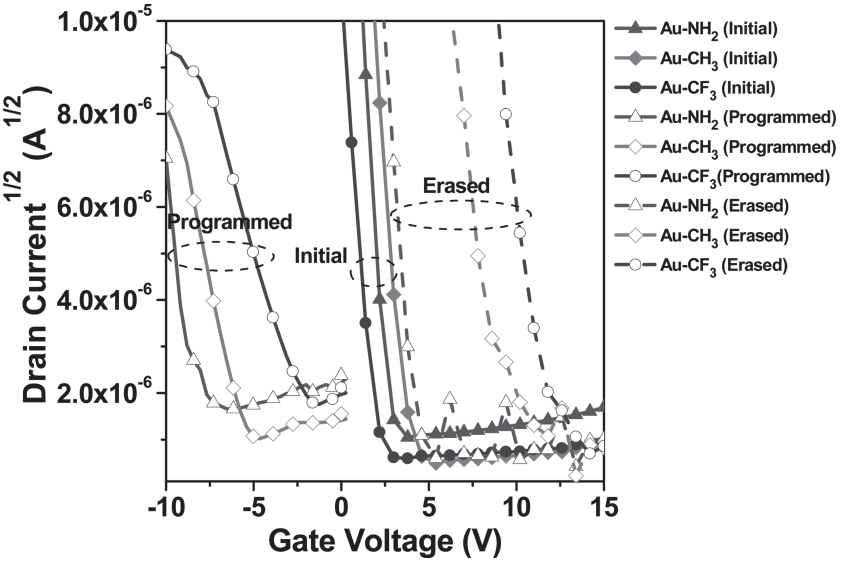

Figure 3. Plot of $I_{ds}^{1/2}$ versus V_g curves of the P3HT:Au NPs nanofiber based transistor memory devices (programmed state: V_g = –5 V, 1 ms; erased state: V_g = 5 V, 1 ms; at a fixed V_d = –5 V).

aluminum oxide (Al_2O_3) used as dielectric layer, having a nominal thickness of 100 nm, were deposited on the top of substrates. Precise control on the diameters (≈120 ± 7 nm) of electrospun nanofiber is achieved by optimized processing parameters. Note that only single hybrid nanofiber is placed on bottom of source/drain electrode (from optical microscopy; Figure S2, Supporting Information). Besides, the observed functionalized Au NPs are located discretely inside the nanofiber or on the surface (from TEM image of Figure 2). The charge carriers of the 1D nanofiber channel with controllable Au NPs can be regulated via applied gate voltage field. A fixed doping concentration of the Au NPs in the collected single P3HT nanofiber matrix is systematically used for comparing the memory switching behavior based on three different SAM modifications.

2.2. Memory Characteristics Based on Hybrid Nanofiber OFETs

The hyrbid nanofiber based OFETs memories were characterized with the gate response at room temperature and in a N_2-filled glove box to eliminate the effect from moisture. The electrical characteristics of OFETs prepared from P3HT-only nanofiber (without Au NPs) on the octadecyltrichlorosilane (ODTS)-modified Al_2O_3/PEN substrate show good p-type characteristics with an ON/OFF current ratio of ≈10^4 (Figure S3, Supporting Information). No hysteresis in transfer curves is observed, suggesting that under the gate voltage (V_g) range negligible charge traps inside the P3HT or at the interface between P3HT semiconducting nanofiber and hydrophobic-treated dielectric. To resolve the Au NPs showing the detectable electrical response, programming/erasing of nonvolatile charges was performed with charging gate voltage pulse of –5 V/5 V for 1 ms. The transfer characteristics (I_d (drain current)-V_g curve) sweeping from 15 V to –10 V at the reading drain voltage bias (V_d) of -5 V based on P3HT:SAM-Au hybrid electrospun nanofiber OFETs are shown in Figure S4 (Supporting Information), and the typical memory operation ($I_d^{1/2}$ versus V_g sweep; **Figure 3**) at initial scan (solid lines with solid symbols) were performed to determine the threshold voltage. Similar to the P3HT-only nanofiber OFETs, all P3HT/Au hybrid nanofiber devices exhibit p-type semiconducting modulation as a negatively increasing gate bias simultaneously increases the nanofiber conduction (initial curves). Precise control on depletion/enhancement mode of OFETs governs the degree and direction of threshold voltage shift. The P3HT:Au hybrid nanofiber OFETs show a negative shift of transfer curve by applying a programmed gate pulse (solid lines with open symbols; Figure 3). This change in threshold voltage by parallel shift of the $I_d^{1/2}$–V_g curve indicates that the negative electrical pulse generates a certain amount of charges trapped in the SAM-Au NPs. Furthermore, the negative direction of threshold voltage shift confirms that effective charges have a positive polarity. Intriguingly, the operation mode of the device switches from the programmed state to erased state (dash lines with open symbols; Figure 3) in a more positive direction with respect to the initial curves after a positive gate bias pulse (5 V for pulse width of 1 ms) is applied. The memory ratio between the electron charged (erased) and hole charged (programmed) state with four orders of magnitude difference determines the bistable switching behaviors of the hybrid nanofiber transistor memories. Besides, more than 5 independent device cells were performed with small variations on cell-to-cell characteristics and good reproducibility.

Electrical output curves (Figure S5, Supporting Information) show well-defined linear and saturation regions in the range of V_d bias applied (between 0 and –5 V). The incorporation of the SAM-Au NPs in the P3HT nanofiber is accompanied by a slight decrease of the drain current. The field-effect mobility in 1D nanofiber is recorded from transfer curves in saturation region at V_d = –5 V and calculated from the slope of a line drawn through the linear part of an $I_d^{1/2}$ versus V_g at initial curves (Figure 3) using the following modified equation.[33]

$$\mu = \frac{d(I_d^{1/2})}{dV_g}\frac{L^2}{C} \quad (1)$$

where μ is the field-effect mobility; L is the channel length; C is the gate capacitance (Equation 2) calculated from the cylinder on a planar substrate for 1D fiber or wire device analysis.[33,34]

$$C = \frac{2\pi\varepsilon_0\varepsilon_r L}{\ln(4h/d)} \quad (2)$$

Here, ε_0 is the permittivity of free space, ε_r is the dielectric constant of gate insulator (9 for Al_2O_3), h (≈100 nm) is the thickness of oxide layer and d (≈120 ± 7 nm) is the nanofiber diameter. **Table 1** reports the average field effect hole mobilities of at least 5 transistors for each hybrid nanofiber. The transistor parameters of the P3HT/Au NPs hybrid nanofiber device can be as high as that of pure P3HT nanofiber with estimated

Table 1. Summary of the electrical properties of hybrid nanofibers based transistor memories.

	Mobility [$cm^2 V^{-1} S^{-1}$]	ON/OFF ratio	Initial V_{th} [V]	Programmed V_{th} [V]	Erased V_{th} [V]	ΔV_{th} [V]	Stored Charge Concentration [charges NP^{-1}]
P3HT	6.13×10^{-2}	7.3×10^4	0.3	—	—	—	—
P3HT:Au-CF_3	5.09×10^{-2}	1.3×10^4	2.3	–1.2	12.3	3.5	18
P3HT:Au-CH_3	4.13×10^{-2}	7.8×10^3	4.1	–5.0	10.2	9.1	47
P3HT:Au-NH_2	3.38×10^{-2}	3.4×10^4	3.3	–7.3	5.0	10.6	54

carrier mobilities of (3–6)×10^{-2} cm^2 V^{-1} s^{-1} and corresponding current ON/OFF ratios of (1–8)×10^4. It indicates that the small fractions of Au NPs (≈3 wt%) in the hybrid nanofiber do not permit a large scale phase separation or disrupt conjugated polymers chain orientation and thus provide percolating charge transport pathways.

Table 1 lists all electrical properties of hybrid P3HT/SAM-Au NPs nanofiber based transistor memories. The quasi-neutral threshold voltages of hybrid nanofiber transistors, defined as the threshold voltage without any charges trapped in Au NPs, are ≈2.3, 4.1 and 3.3 V for Au-CF_3, Au-NH_2, and Au-CH_3 SAM, respectively. As the gate bias is negatively applied, the gate voltage (when the transfer curve started negatively shifting) is interpreted as the programmed state threshold, which is originally considered to be from the tunneling of the charges between Au NPs and P3HT nanofiber channel. Large threshold voltage shifts (≈V_{th}) of ≈3.5, 9.1 and 10.6 V are observed for Au-CF_3, Au-CH_3, and Au-NH_2 SAM, respectively. The total numbers of the stored charges are approximately given by the relationship between threshold voltage shifts and charge numbers in each Au NPs:[11,35]

$$\Delta V_{th} = \frac{q n d_{NPs}}{C} \quad (3)$$

Here, q and d_{NPs} are the magnitude of the electron charge and density of Au NPs (≈10^{-11} cm^{-2} from TEM images in Figure 2). From the Equation 3, stored charge concentrations (n) are 2.8 × 10^{12}, 7.1 × 10^{12}, and 8.2 × 10^{12} charges cm^{-2} within nanofiber based on Au-CF_3, Au-CH_3, and Au-NH_2, respectively, i.e., about 18, 47, 54 charges per NP. More trapped charges detected are attributed to the geometrically high surface area to volume ratio of the hybrid nanofiber, which are one order of magnitude higher than that of the reported Au NPs-based nano-floating gate OFETs.[9–14] The threshold voltage shifts to the negative directions with respective to those of the quasi-neutral state are mainly due to the hole injection from the 1D nanofiber channel into the embedded Au NPs.

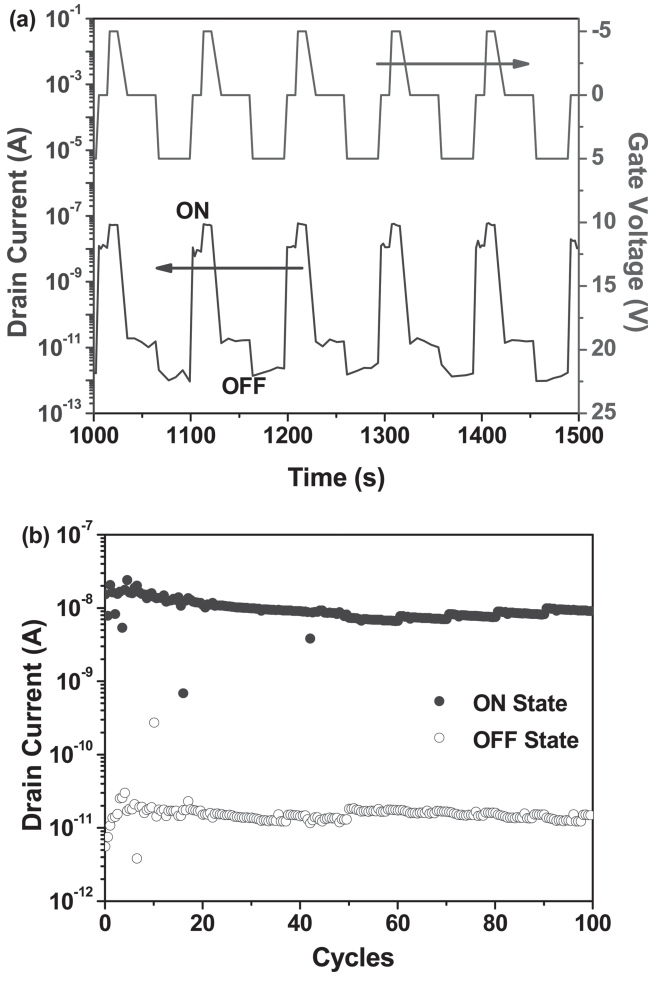

Figure 4. a) WRER cycles and b) Endurance characteristics of P3HT:Au-CF_3 hybrid nanofiber based transistor memory device.

The stress endurance of the hybrid nanofiber transistor memories by applying ± 5 V programmed/erased pulses is shown in the write-read-erase-read (WRER) cycles (**Figure 4**a). Typical P3HT:Au-CF_3 nanofiber OFETs exhibit reversible and stable switching behaviors between the ON and OFF states, with the conductance change of nearly 2.6 ×10^3 (at zero gate bias) being maintained for at least 100 cycles, indicating the good stress endurance characteristics (Figure 4b). Au-CH_3 and Au-NH_2 based hybrid nanofiber transistor memories can also be switched for 100 cycles without a significant change in the memory ratio (Figures S6 and S7, Supporting Information). To judge the nonvolatility of the programmable memory switching, the device retention time defined as the time duration of the charge stored in the Au NPs without leakage is characterized. **Figure 5** shows the plots of I_d vs. time for P3HT:Au-CF_3 hybrid nanofiber device in the ON (solid circles) and OFF (open circles) state measured at a time interval of 10 s at V_g = 0 V and V_d = –5 V after performing the erased/programmed operation for 1 s. The initial ON/OFF ratio exceeds 10^4 but the ON or OFF current slightly decreases with time; however, this difference in both current states still maintains for at least 10^4 s. The device with Au-NH_2 shows a relatively slow decay in the ON state

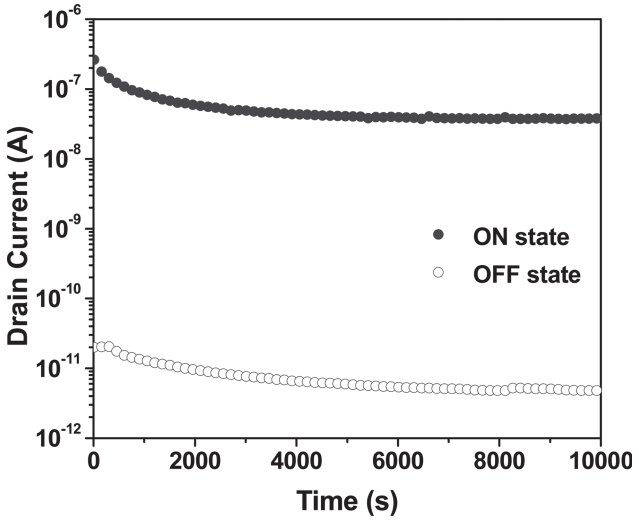

Figure 5. Retention time test of the P3HT:Au-CF_3 hybrid nanofiber based transistor memory device.

current and a slow increase in OFF state current (Figure S8a, Supporting Information) while both ON and OFF currents of Au-CH_3 device nearly keep a constant (Figure S8b, Supporting Information). Basically, these results suggest that all SAM modifications on Au NPs are critical molecules in efficient charge storages and the nonvolatility of the hybrid nanofiber transistor devices ensures the practical memory device platform.

2.3. Hybrid Nanofiber Transistor Memories Under Bending Conditions

As a next step, the development of next-generation organic memory device relied on not only the good performance but also device fabrication on the bending flexible substrate. Our P3HT:Au NPs hybrid nanofiber based transistor memories on the PEN substrate are physically flexed with a vernier caliper from flat to bending condition (see **Figure 6**a). The hybrid nanofiber memory device architectures are not cracked or deformed upon the bending due to the high ductility of the Au electrode coupled with nanofiber channel. The statistical data on threshold voltages under programmed/erased state, mobility and ON/OFF state current of the flexible transistor memories with various bending radii or repeated cycles are discussed in the following. In each condition, standard deviations calculated from 5 data of critical performing parameters were statically analyzed. Accordingly, hybrid nanofiber memory device show excellent mechanical properties under the bending test regardless of the ligands of functionalized Au NPs. The programmed/erased threshold voltage (Figure 6b) and mobility (Figure 6c) are analyzed at various curvature radii of 30, 20, 10 and 5 mm. Negligible changes in the device characteristics are observed even at a bending radius as small as ≈5 mm. All the mobility levels of the transistor memories remain similar without any notable fluctuation. The bending stability of hybrid nanofiber memory devices is further examined as a function of numbers of bending cycles (**Figure 7**). This test is performed by means of repetitive substrate bending/spreading from flat plane to severest bending condition (≈5 mm bending radius) at a rate of 2 bends s^{-1}. The recorded programmed/erased threshold voltages are negligibly changed and the ratios of ON to OFF drain current show virtually no change during the 1000-bending cycle test. It reveals that our flexible hybrid nanofiber device have good mechanical flexibility as well as programmable memory endurance.

2.4. Switching Mechanism

The role in electronic transport and trapping are used to understand the switching mechanism on the hybrid nanofiber transistor memories.[9–13,32] Hole trapping at the defect of the P3HT or interface between gate dielectric/P3HT can not be responsible for non-hysteresis kinetics of pure P3HT nanofiber device (Figure S3, Supporting Information). A charge trapping site may donate a majority carrier (hole in the case of P3HT) to the conduction state but the remaining opposite charges is possible to be localized on the trapping site. Therefore, in our case, ≈10 nm sized Au NPs is used as the high density and discrete charge elements. The charges responsible for the switching behavior used to configure a three-terminal memory would be spatially separated from the interface; thus, similar to be created and trapped. Charge traps at the P3HT/Au NPs interface influence the accumulated density of holes. The schematic diagrams of switching mechanism are illustrated in **Figure 8**. The holes induced in the P3HT nanofiber channel at negative gate voltages transfer into the Au NPs trapping interface via Fowler-Nordheim (F-N) tunneling.[36,37] The extracted charges cannot be returned for a long time due to the valence band offset built up at the interface between P3HT and SAM-Au NPs.[32] Conversely, when a reverse positive pulse is applied, the detrapping process can occur due to the back transfer of holes to the P3HT or recombination with trapped opposite polarity charge carriers. The charging/discharging procedure of Au NPs affects enhancement/depletion mode of OFETs, thereby leading to the conductance change and threshold voltage shifting.

Trapping sites, as well as electrical bistability with threshold voltage shifting in the memory devices, could be manipulated efficiently by tuning the size,[13] doping concentration[10,11,16] and surface modifications[32] of the metal NPs. For Au NPs-based nonvolatile organic transistor memories, the threshold voltage shifting in programmed/erased states has a strong size-dependence since bigger size Au NPs traps much more charge carriers due to its lower charging energy with interparticle hole conduction.[13] In our device, the size effect based on different SAM-Au NPs trapping sites is excluded according to a fixed Au NPs density. Trapping of either charge at surface states is strongly related to the affinity of the SAM derived from organic thiolate ligands on the Au NPs. Short alkyl-chain modification possibly contributes a fast response to switching action.[32] The transistor memories reported above were generally obtained from OFETs based memory devices in thin film state.[9–16,32,36] Here, Au NPs-containing memory devices composited of electrically active constituents are fabricated by using 1D

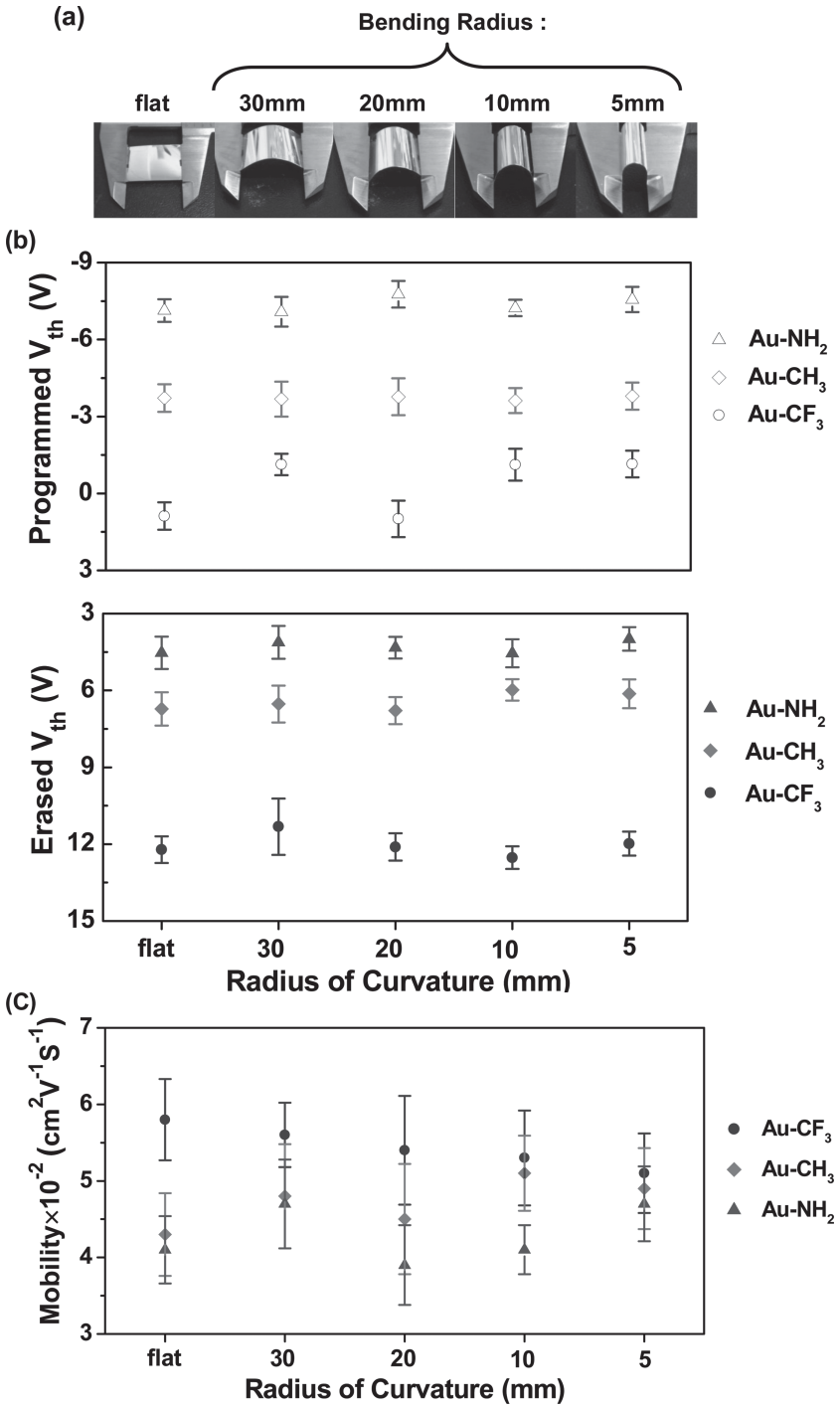

Figure 6. a) Hybrid nanofiber based transistor memory devices under flat and various bending radii. b) Variation of programmed and erased threshold voltages of the flexible hybrid nanofiber based transistor memory devices. c) Variation on the mobilities of the flexible hybrid nanofiber based transistor memory devices.

P3HT nanostructured fiber-like channel. Charge carriers are confined in 1D nanofiber that can enhance/modulate the channel conductance, resulting in a good propagating transportation. Therefore, P3HT/SAM-Au NPs hybrid nanofiber has the correspondingly increased surface area through the non-planar channel geometries and high electric fields at nanofiber/dielectric surface[22,27,38] without inserted thick dielectric tunneling barriers compared to planar thin film channel. It suggests that the holes are efficiently injected into the SAM-Au NPs from P3HT in the nanofiber and remained trapped until the reverse polarity. Large charge storage capacities and long charge retention characteristics of the fabricated hybrid nanofiber device explain the confinement on charge-trap Au NPs sites through 1D nanostructured channel.

Au NPs with different electron affinities are also likely the major effect on the switching of the hybrid nanofiber transistor memories via changing the surface ligands. The surface properties of Au NPs affect the interfacial characteristics such as density and surface potential of trapping sites. The efficiency of charging is possibly reflected in the observed threshold voltage shifting, becoming larger if more charges are retained. The greatest negative threshold voltage shift is observed in the Au-NH_2 based hybrid nanofiber device, which is attributed to the polarity of functionalized Au NPs surface. Different nature of the SAM chemisorbed on the Au NPs surface also influences the modulation of charge tunneling barriers.[32,39] SAM on Au NPs with terminal perfluorinated and amine groups have opposite trends in dipoles to increase and decrease the Au NPs work functions, respectively.[39] Therefore, increasing Schottky barrier (mismatch of energetic levels) of the P3HT:Au-CF_3 hyrbid nanofiber device slows down the charge trapping process, suppressing the threshold voltage shift. Conversely, a lowered working function of the Au-NH_2 eliminates the hole injection barrier between P3HT/Au-NH_2 and facilitates charge transport and trapping of holes from P3HT to NPs. Therefore, the hole trapping effect of the Au NPs embedded in the p-type P3HT nanofiber contributes to the decrease in drain current and threshold voltage shifting more negatively in the following the order: Au-NH_2 > Au-CH_3 > Au-CF_3.

Toward high density and low power consumption nonvolatile solid state storage devices, the combination of 1D nanostructured conductance channel and SAM-modified NPs could meet continuous device scaling although it still remains challenging. It is worth noting that our direct fabrication approach can

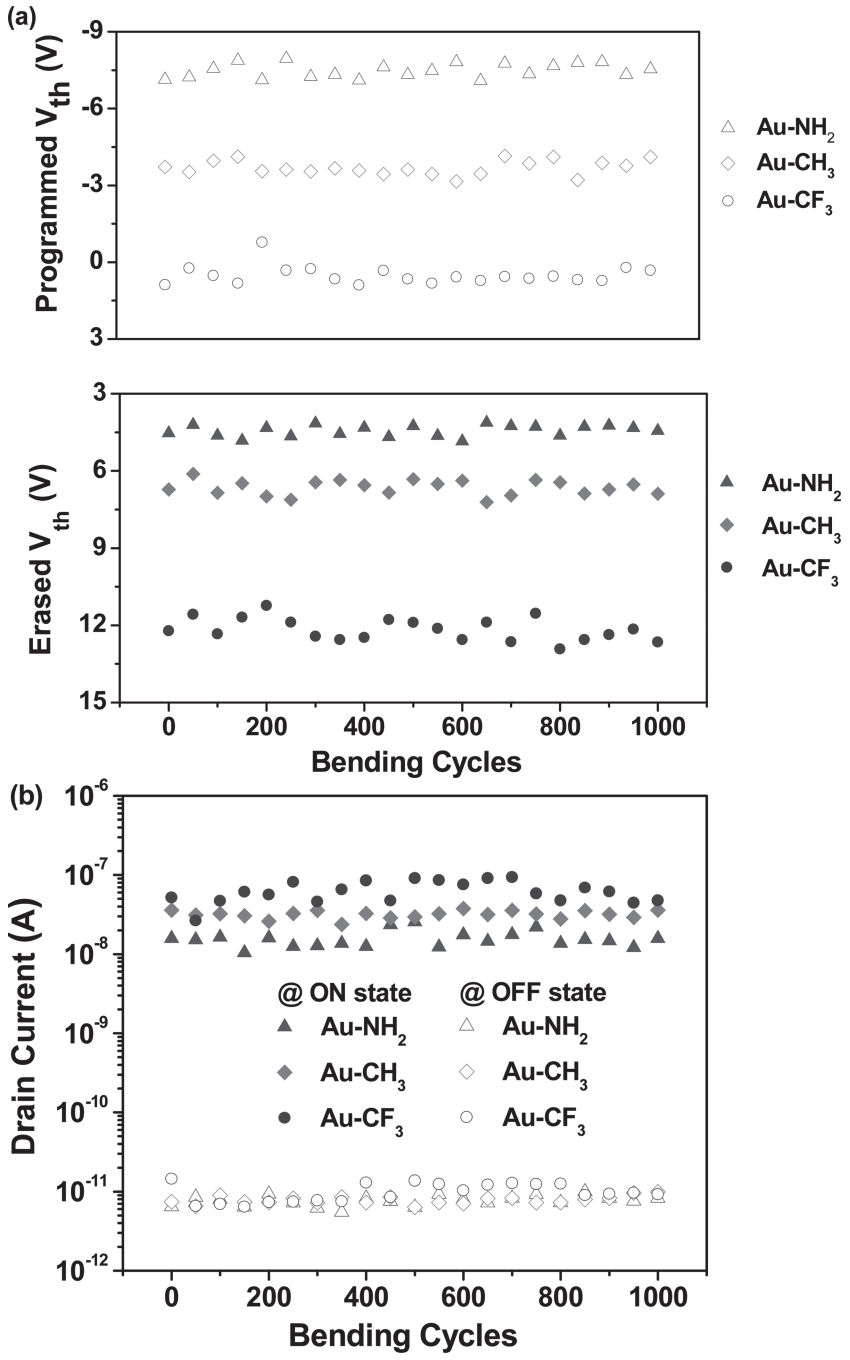

Figure 7. a) The programmed/erased threshold voltage and b) the drain current of the flexible hybrid nanofiber based memories as a function of the number of bending cycles.

work under relatively low operation voltages (±5 V) that have possibly practical applications for standard semiconductor integrated circuits. The memory device would not have any requirement to supply too much operating power voltage resulting in a low energy consumption. The combination of 1D hybrid nanofiber channel geometries with a high electric field and an ALD layer of high-k Al_2O_3 dielectric would certainly facilitate the charge injection into the storage layer as well as fast and significant charge trapping. With this state-of-the-art approach, controllable density and alignment of 1D hybrid nanofiber device with reproducible memory properties can be integrated into large area mechanically flexible circuits.

3. Conclusions

In conclusion, flexible organic memories consisted of P3HT electrospun nanofiber transistors functionalized with surface-modified Au NPs have been assembled. The electrospun hybrid nanofiber enabled low-temperature and simple fabrication on flexible substrate with an excellent mechanical stability. Of these, hybrid semiconducting nanofiber channel and metal NPs as potential wells result in the charge being stored or erased by applying appropriate gate voltage. The threshold voltage shift of the transfer curves between programmed/erased states indicates that holes in the P3HT nanofiber are transported to the localized trap sites by the Au NPs surfaces modified with terminal CF_3, CH_3 and NH_2 group, which can be structurally related to the memory performance. Typical as-fabricated P3HT:Au NPs hybrid nanofiber transistor memories have low operation voltages of ±5 V, large threshold voltage shifts of 3.5–10.6 V, long retention ability of up to 10^4 s and good stress endurance of at least 100 cycles. These merits further suggest that the hybrid semiconducting electrospun nanofiber could be potentially used advanced flexible nonvolatile memory devices.

4. Experimental Section

Au NPs Synthesis: Functionalized Au NPs were synthesized by a single-phase reduction reaction, according to the Brust-Schiffrin method.[40] Typically, hydrogen tetrachloroaurate trihydrate (234 mg, 0.59 mmol) and ligands (282 mg, 1.8 mmol) were dissolved in methanol (150 mL). Then, acetic acid (10 mL) was added to the mixture, and 30 mL of freshly prepared 0.4 M aqueous sodium borohydride was added carefully in one portion with vigorous stirring. The color of solution mixture turned into wine-red immediately indicating the formation of gold clusters with the size range around 15 nm. After further stirring for 30 min, the solvent was removed under reduced pressure, and the residue was washed thoroughly with diethyl ether to remove excess ligands and with water to remove borates and acetates. The product was dried under a stream of N_2, followed by a final drying on a vacuum line. Finally, 132 mg of the pure products as a wine red solid was obtained.

Electrospinning Process: A two-fluid coaxial electrospinning system with modified collector was used to produce core-shell nanofiber.[30] The

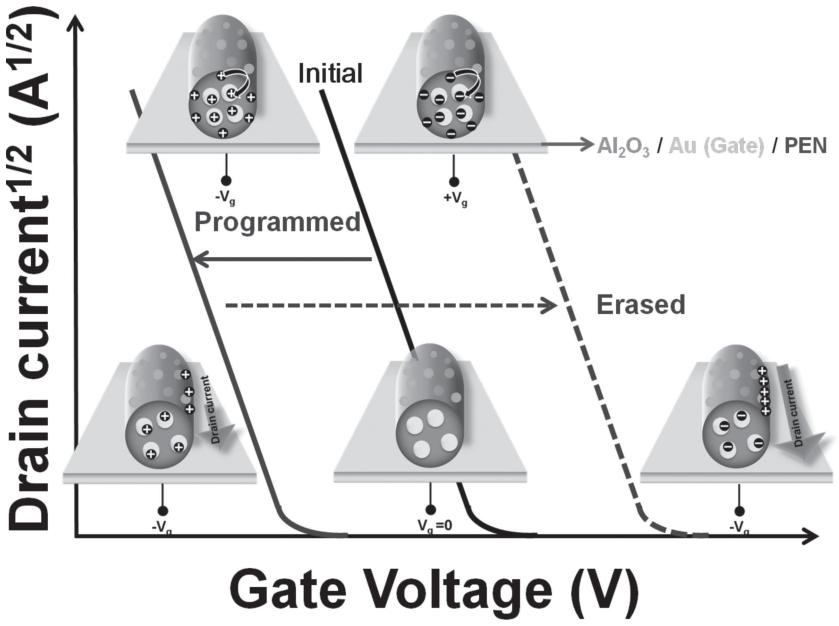

Figure 8. Schematic diagram on switching mechanism of the P3HT:Au hybrid nanofiber based transistor memory devices.

core and shell precursor solutions in the two syringes were used for preparing electrospun nanofiber. Note that each syringe was connected to the separate needles for two-fluid coaxial electrospinning system. Au NPs (3 wt%):P3HT (50 mg mL^{-1}) hybrid mixture in chlorobenzene as core solution was dissolved in anhydrous chloroform overnight in the N_2-filled glovebox. PMMA was also dissolved in anhydrous chlorobenzene (300 mg mL^{-1}) with 10 wt% of TBAP added to increase conductivity and stabilize the cone-jet (used as shell solution). The two solutions were fed into the coaxial capillaries by two syringe pumps (KD Scientific Model 100, USA). The feed rate of P3HT:Au NPs solution (core flow) was at 0.1 mL h^{-1} and the feed rates of PMMA solution (shell flow) was at 1.0 mL h^{-1}. The tip of the core needle was connected to a high-voltage power supply (chargemaster CH30P SIMCO, USA) with the voltage of 10.1 kV. The collector made of electrically charged conductive aluminum disk (diameter: 7 cm) with a rectangular hole (4 cm in length and gap width of 1 cm) was placed under the tip of the needle (working distance: 13 cm) to collect the nanofiber. The stable cone-jet spinning mode in the electrospun process system was monitored by CCD camera (Xli 3 M USB 2.0 CCD camera, USA) and Macro video zoom lens (OPTEM MVZL, USA) for obtaining uniform nanofiber. All electrospinning experiments were carried out under ambient environment.

Characterization: The optical properties of Au NPs solutions were evaluated in chloroform using UV-Vis spectroscopy (JASCO V-670). X-ray photoelectron spectroscopy (XPS) measurements were collected using VG ESCA Scientific Theta Probe spectrometer. The morphology of the prepared P3HT ES hybrid nanofiber was characterized by the transmission electron microscope (TEM, JEOL 1230).

Device Fabrication and Measurement: The flexible PEN with a 100-nm-thick Au gate electrode was subsequently deposited by thermal deposition, then using atomic layer deposition (ALD) method to prepare 100-nm-thick Al_2O_3 as dielectric. The Al_2O_3/PEN substrates were treated with ozone plasma for 5 min, and then the substrates were immersed into 10 mM octadecyltrichlorosilane (ODTS) in anhydrous toluene for 2 h. The coaxial P3HT:Au NPs (core)/PMMA (shell) electrospun hybrid nanofiber was transferred from collector onto the ODTS-modified Al_2O_3/PEN substrate. For the purpose of immobilization, the electrospun hybrid nanofiber on the substrate was immersed in acetone for 30 min to extract the PMMA shell layer and then dried under vacuum. Thick gold source/drain electrodes (30 nm) were thermally deposited through a regular shadow mask with the channel length (*L*) and width (*W*) of 25 and 1500 μm, respectively. The measurement of the top-contact bottom-gate transistor memories characteristics for the fabricated P3HT:functionalized Au NPs hybrid nanofiber devices was carried out at room temperature using Keithley 4200-SCS semiconductor parametric analyzer in a N_2-filled ambient.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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